PlatformConference

Direction • Design • Perspective • Analysis

High Performance Programmable Solution for HyperTransport™ Technology

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XILINX®

The Programmable Logic Company℠

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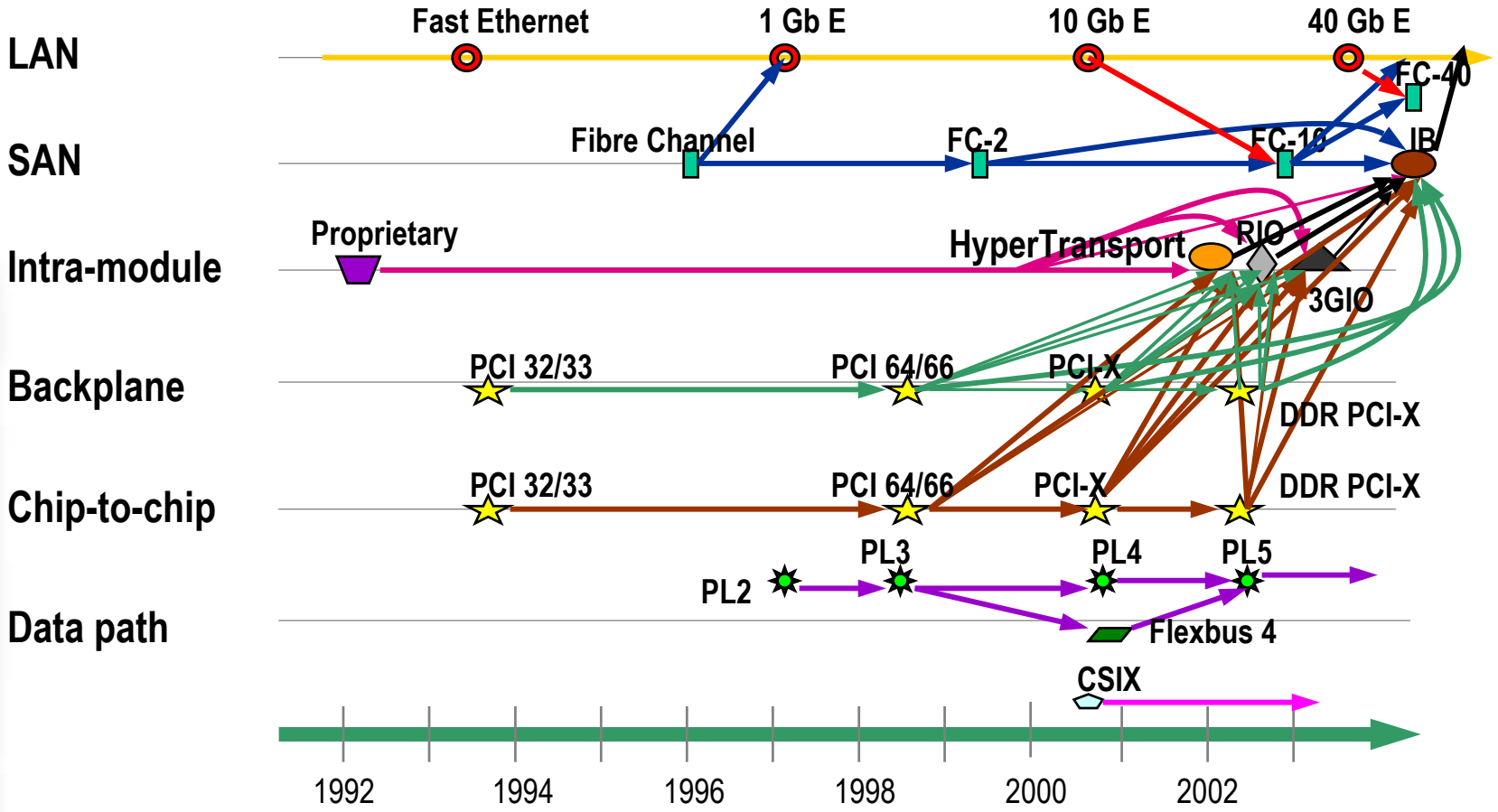
Explosion of New Connectivity Standards



A typical Terabit System will use two or more standards at a time!

Increased Usage of Future-Proof Programmable Solutions

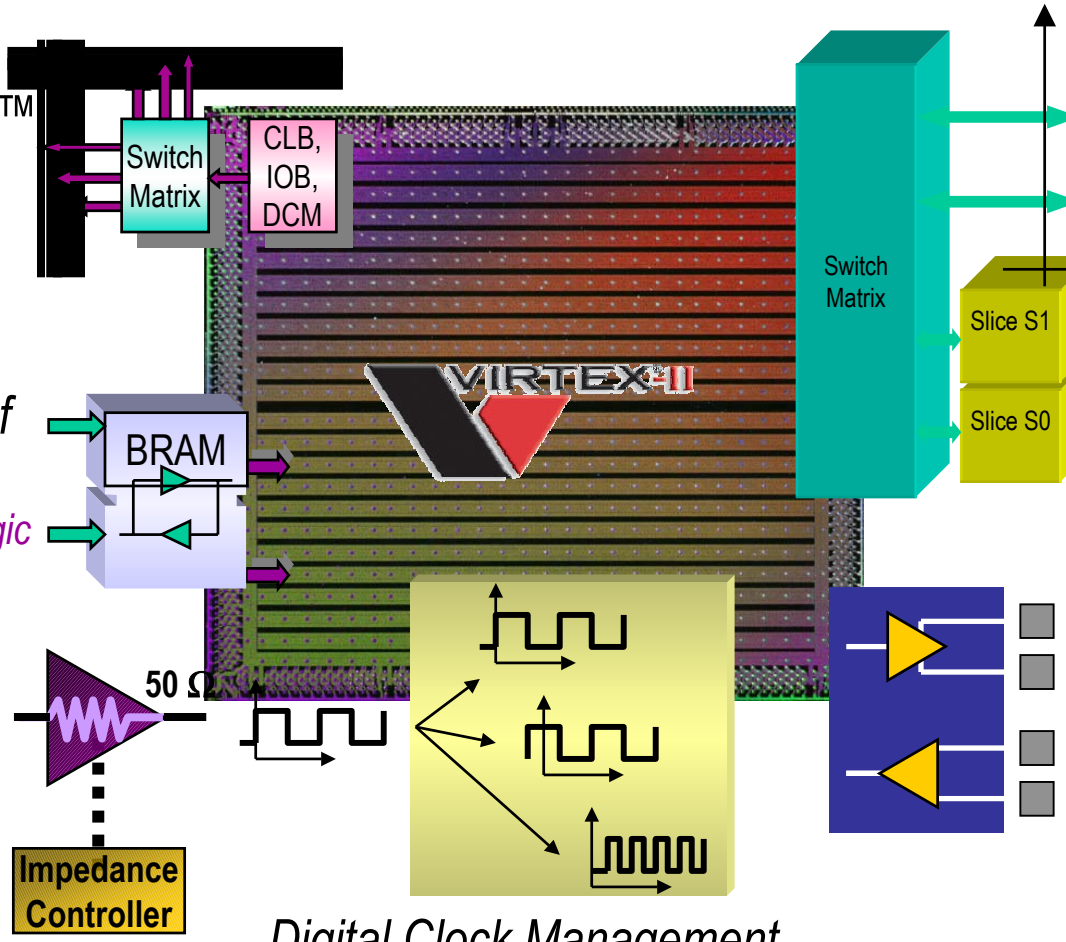
- Service providers and enterprises are looking to extend product life cycle and ROI
  - Field upgradeability allows product future-proofing
- Equipment manufacturers are looking to lower design risk by using “off-the-shelf” solutions
  - Allows adapting to evolving standards & changing specs
  - NPUs - customized functionality through C-code
  - FPGAs - customized functionality through HDL

Platform FPGA Value Propositions

Active interconnect™ Technology
Fast, predictable routing delays

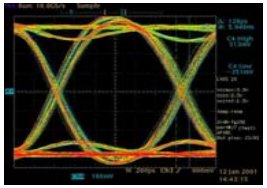
Abundances of On-chip RAM
Fast & efficient logic
Highest flexibility

On-chip termination
Improved signal integrity
Reduced lay-out complexity



Powerful CLB
>300 MHz Performance

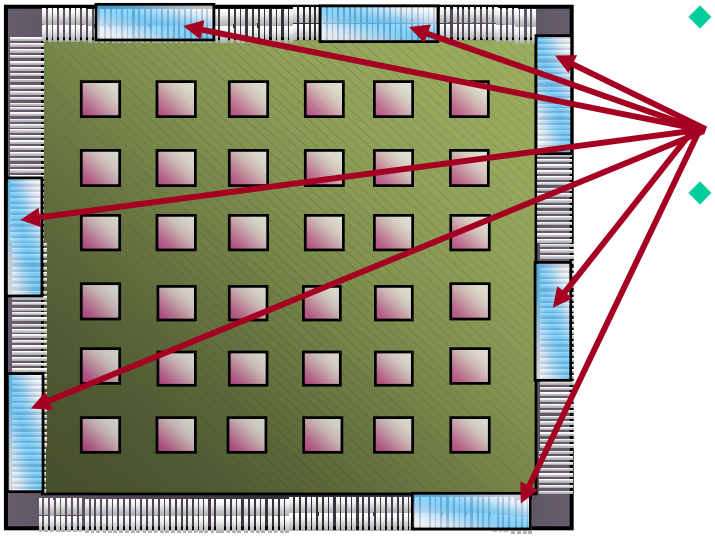
Programmable I/Os with LVDS
(840 Mbps Eye)



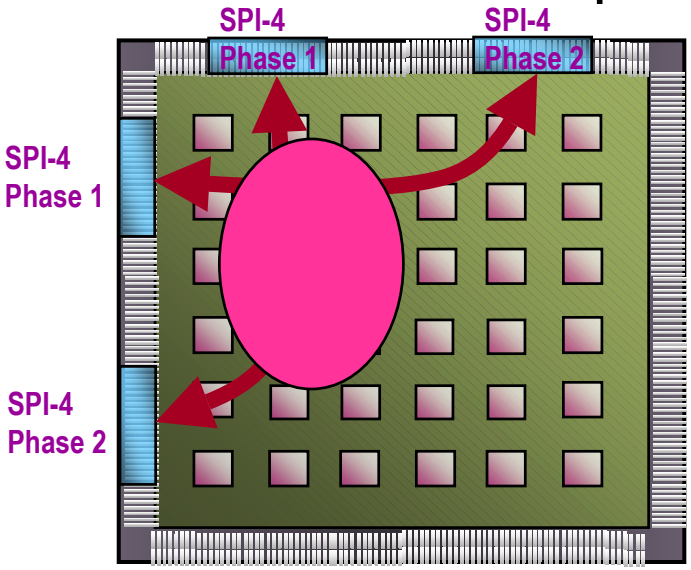
Digital Clock Management
Precise frequency generation and phase control
Managing both on-chip & off-chip clock synchronization

Flexible 840 Mbps LVDS Solution

First to Combine Flexibility and Scalability with Guaranteed Performance



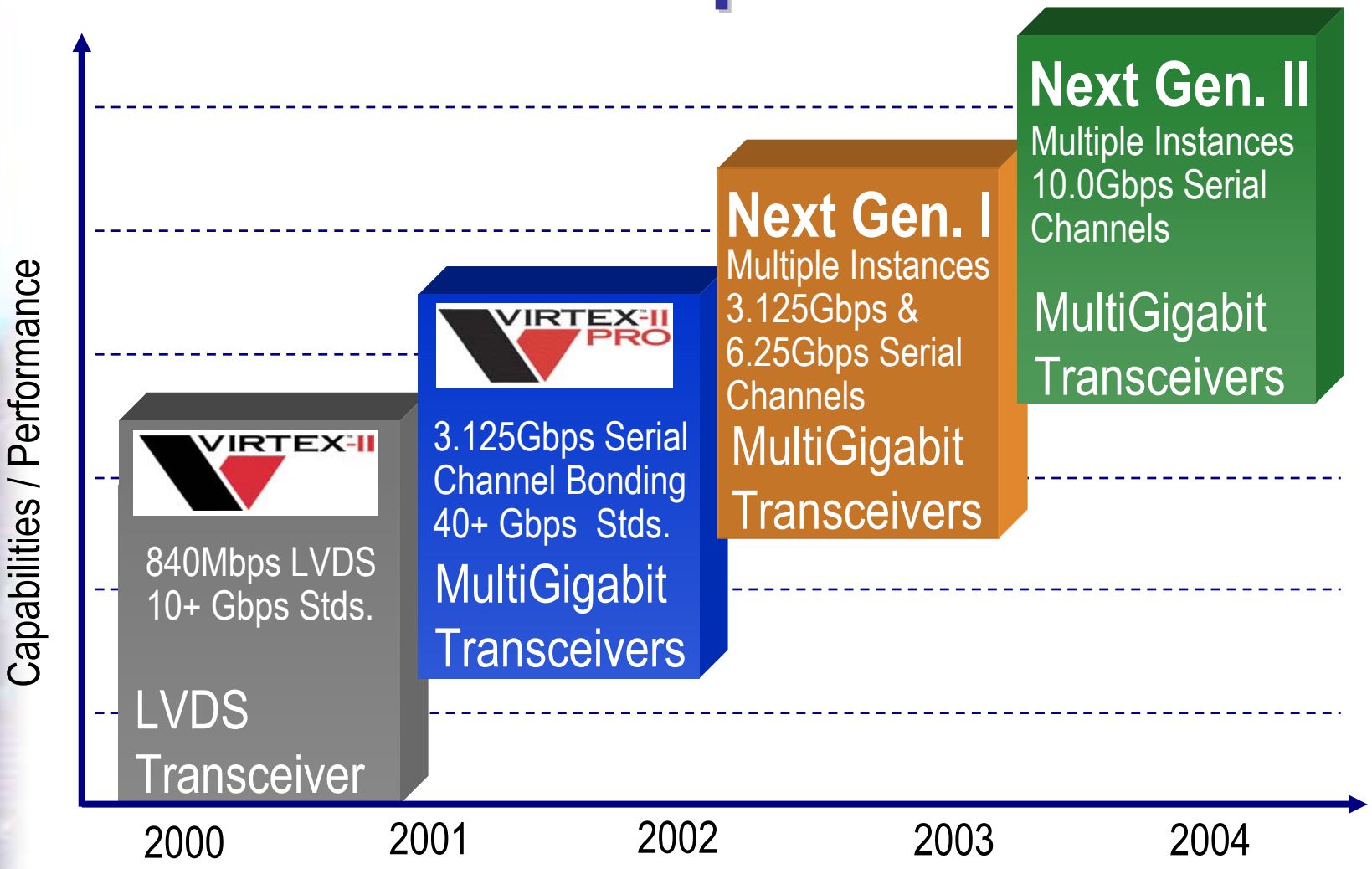
- Can be placed anywhere in the chip
- Allows 7 transmit/receive implementations of 16b LVDS busses on one chip



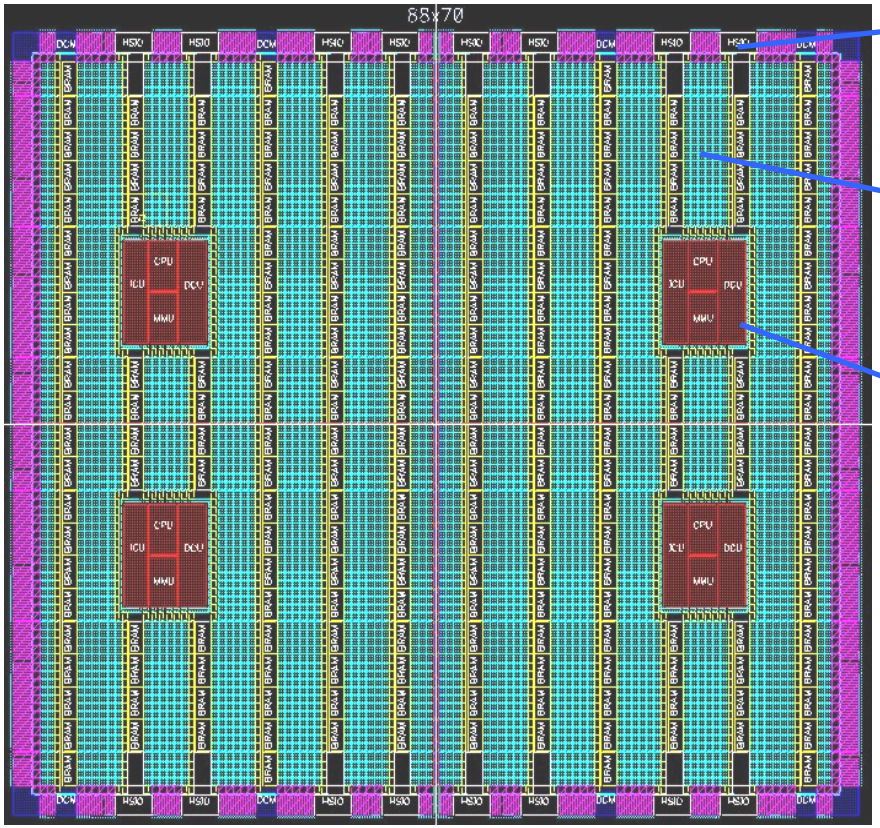
Usage examples

- High speed interface between NPU and traffic manager
- Four instances of SPI-4 cores can be used to build a switch

From 840 Mbps LVDS to 10 Gbps Serial



PowerPC & Multi-Gigabit Transceiver Synergy

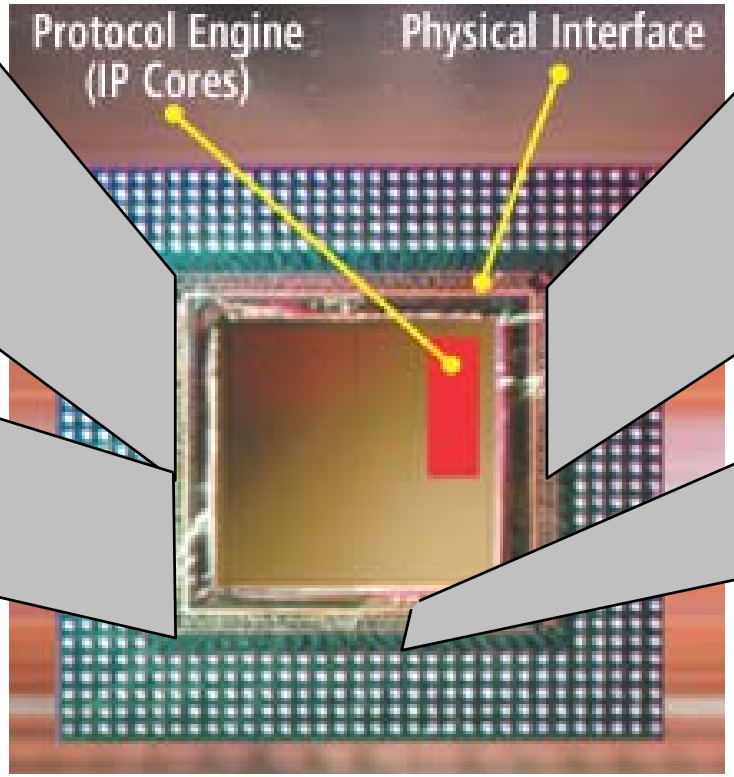


Transceiver is PHY

Fabric is MAC/Link

Protocol Stack Runs on PowerPC

Platform FPGA SystemIO Solutions



System-Synchronous Parallel

- PCI 32,64-bit 33/66
- PCI-X 64-bit, 100

Source-Synchronous Parallel

- RapidIO™
- HyperTransport™
- POS-PHY™ L3 & 4
- FlexBus 4™
- 1 Gigabit MAC w/ GMII
- 10 Gigabit MAC w/ XGMII
- CSIX-L1

Advanced Memory Interfaces

- ZBT SSRAM
- DDR SDRAM
- QDR SSRAM
- CAM

High-Speed Serial (Next Generation)

- Multi-Gigabit Backplanes
- Infiniband™
- Gigabit Ethernet PHY
- 10 Gigabit Ethernet PHY(XAUI)
- Fibre Channel
- 3GIO
- Serial ATA
- RapidIO Serial

SystemIO = Protocol Engine (IP Cores) + Physical Interface(SelectI/O-Ultra™ technology)

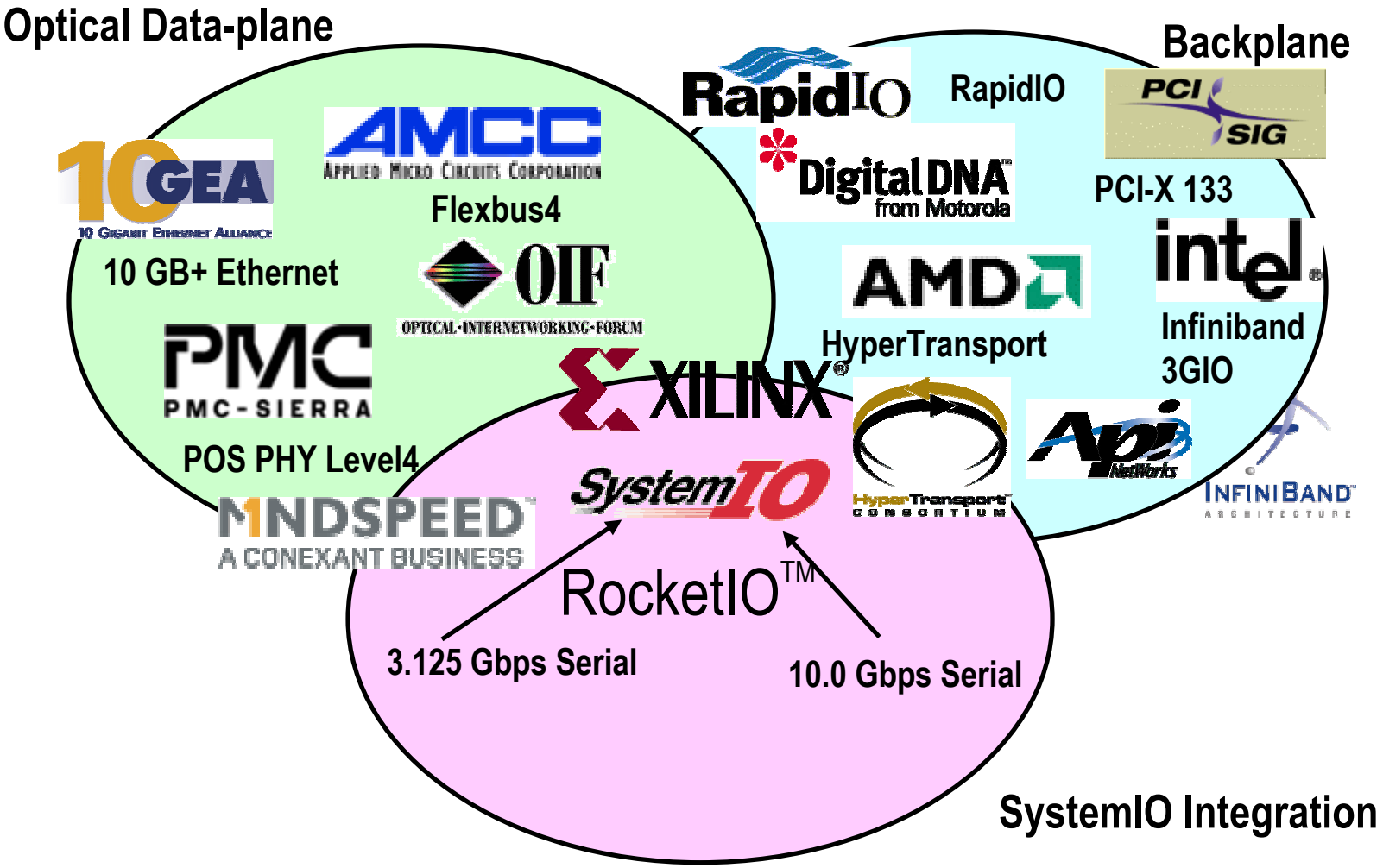
SystemIO Value Propositions

Design Flexibility and Reduced Risk

- Adapt to emerging standards
- Allow change to evolving std. specs
- Minimize time for “re-spins”
- Allow for future proofing

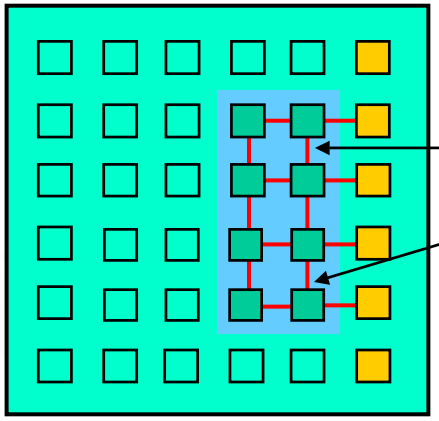
SystemIO Value Propositions

Standards Compliance & Proven Interoperability



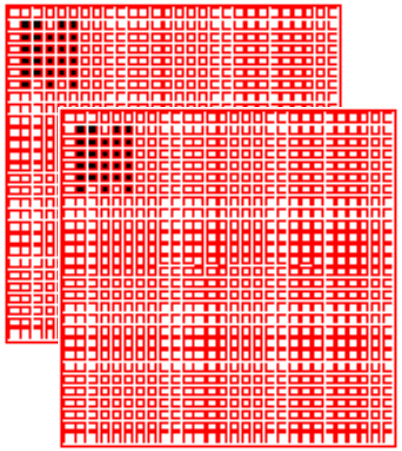
SystemIO Value Propositions

Improved Productivity



- SystemIO IP cores with pre-defined placement and routing
  - Improved predictability
  - Guaranteed performance

- SystemIO pre-verified IP cores advantages
  - Easy drop-in functionality
  - Improved Time-to-Market
  - Reduced Cost



Xilinx Collaborates with Industry Leaders

- Partnership with API NetWorks
  - Joint definition and engineering
  - Verification and optimization of core for Virtex-II
  - API FPGA switch demo based on 2V6000 device
- On SystemIO roadmap for release early ‘02
- Xilinx is a contributor level member in the HyperTransport Consortium

Xilinx® HyperTransport Solution

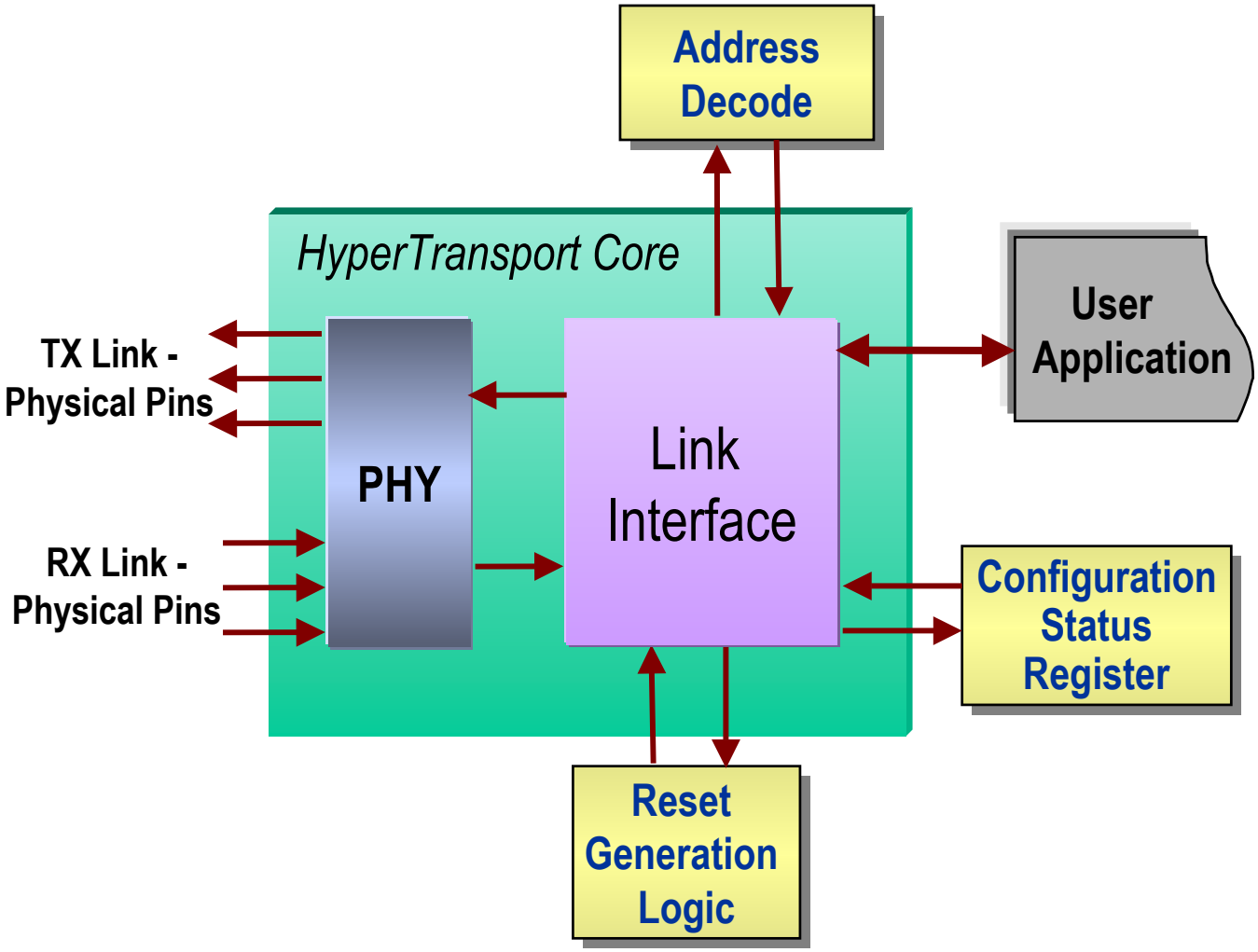
- Product Deliverables
  - Netlists
  - Constraints files
  - Instantiation templates: Verilog and VHDL
  - Datasheet
  - Sample testbench
- Product roadmap
  - Single-Ended Slave = available early ‘02
  - Tunnel and Host on SystemIO roadmap

Single-Ended Slave Core Features

- Bus-width: 8-bit HT link (CAD), 1 CLK & 1 CTL
- Link frequency: 400Mbps (per channel)
  - 200MHz DDR
- Core frequency: 50MHz
- 64-bit internal data path
- 3 virtual channels for core-application interface
  - 64-bit Rx and Tx data paths per virtual channel

Single-Ended Slave Core

Block Diagram

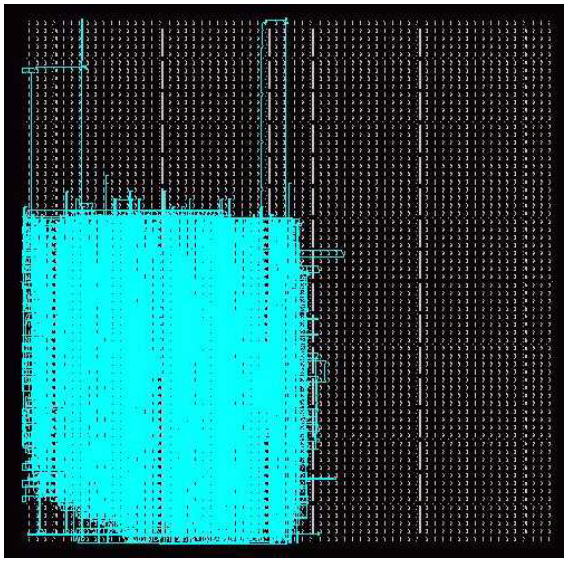


Xilinx supplies reference designs for Address decode, CSR, and Reset logic

Single-Ended Slave Core

Resource Utilization

- Slices: 4300
- BRAM: 7
- Global Clocks: 2
- Uses ~30% of Virtex-II XC2V3000 device



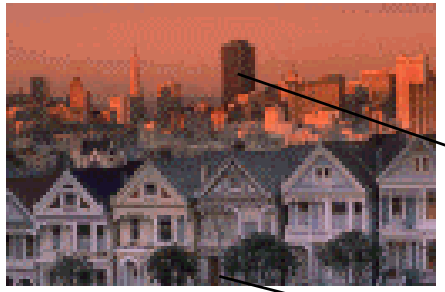
Only Xilinx SystemIO Provides Complete Connectivity Solution

From Chip-to-Chip to WAN

VIRTEX-II

LAN/MAN/WAN

- 10/100 Ethernet
- *1Gb Ethernet*
- ★ 10Gb Ethernet

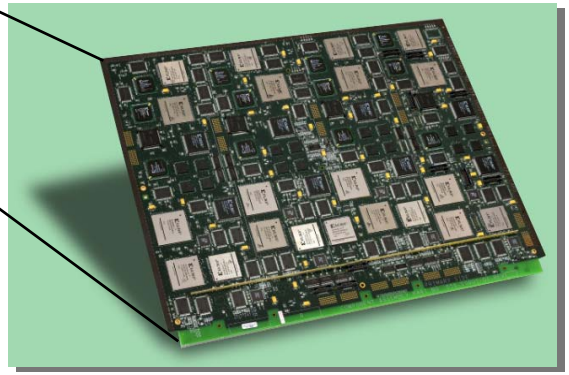


Board-to-Board

- ★ PCI 32/33
- ★ PCI 64/66
- ★ RapidIO
- ★ PCI-X 66 & 100
- *HyperTransport**

Chip-to-Chip

- ★ PCI 32/33
- ★ PCI 64/66
- ★ PCI-X 66 & 100
- ★ RapidIO
- ★ POS-PHY L3 & 4
- ★ Flexbus 4
- ★ CSIX
- *HyperTransport**



★ Semiconductor industry's first!

★ FPGA industry's first

* Available early '02